## REMARKS

This is a response to the Office Action dated April 1, 2004. Claims 1-41 are pending in the application. In the Office Action, the Examiner objected to informalities in the specification. In addition, claims 6-7, 16-17, 29-30, and 38 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Claims 3, 6-7, 16-17, 29-30, 38, and 41 were rejected under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Claims 1-5, 8-9, 11-15, 18-19, 22-28, 31, 34-36, and 39 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,313,586 to Serge Rutman ("Rutman"). Claims 6-7, 16-17, 29-30, and 37-38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rutman in view of U.S. Patent No. 5,870,109 to Joel C. McCormack et al. ("McCormack et al."). Claims 10, 20, 32, and 40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rutman in view of Betty Prince, "High Performance Memories," 1996 ("Prince"). Finally, claims 21, 33, and 41 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rutman.

The rejections from the Final Office Action of April 1, 2004 are discussed below in connection with the various claims. No new matter has been added. Reconsideration of the application is respectfully requested in light of the following remarks.

### I. OBJECTIONS TO THE DRAWINGS

The Examiner objected to the drawings as failing to comply with 37 C.F.R. 1.84(p)(5) because they do not include reference signs mentioned in the description. The Examiner also objected to the drawings as failing to comply with 37 C.F.R. 1.84(p)(5) because they include reference signs not mentioned in the description. With this response, replacement drawings complying with 37 C.F.R. 1.84(p)(5) have been provided for figures 3 and 15. Accordingly, Applicants respectfully request these objections of the drawings be withdrawn.

### II. OBJECTIONS TO THE TITLE

The Examiner objected to the title as not being descriptive. With this response, Applicants have amended the title and respectfully request this objection be withdrawn.

## III. OBJECTIONS TO THE SPECIFICATION

The Examiner objected to the specification for failing to comply with informalities. With this response, Applicants have amended the specification and respectfully request these objections be withdrawn.

## IV. OBJECTIONS TO THE ABSTRACT

The Examiner objected to the abstract for including certain grammatical mistakes. With this response, Applicants have amended the abstract and respectfully request these objections be withdrawn.

## V. REJECTIONS UNDER 35 U.S.C. § 112, first paragraph

Claims 6, 16, and 29 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. In particular, the Examiner noted that a content addressable memory ("CAM") could not be a processor as claimed. Applicants respectfully disagree. As noted in the Free On-Line Dictionary of Computing, a CAM is, "A kind of storage device which includes comparison logic with each bit of storage. A data value is broadcast to all words of storage and compared with the values there. Words which match are flagged in some way. Subsequent operations can then work on flagged words, e.g. read them out one at a time or write to certain bit positions in all of them. *A CAM can thus operate as a data parallel (SIMD) processor.*" (emphasis added) (available at **http://www.foldoc.org/foldoc/foldoc.cgi?content+addressable+memory**). As one of ordinary skill in the art would appreciate the processing capabilities of a CAM, Applicants submit that claims 6, 16, and 29 comply with the enablement requirement and respectfully request that these rejections of these claims be withdrawn.

Additionally, claims 7, 17, 30, and 38 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. In particular, the Examiner noted that the term "classification processor" found in the claims is not well known in the art. Applicants respectfully submit that the term "classification processor" was well known in the art at least as of the filing of Applicants' application. For example, the term "classification processor" is used throughout a press release of IDT of Santa Clara, CA dated April 30, 2001

and titled, "Solidum Systems *Classification Processor* Selected for Transtech Networks Multi-Services Switch" (emphasis added) (available at **http://www.idt.com/news/Apr01/04_30_01_s1.html**). The press release describes some features of a particular classification processor and describes generally the family of classification processors offered by IDT. Similarly, Feliks J. Welfeld noted in "The Case For A Standalone *Classification Processor*," dated October 22, 2002, that, "A recent survey conducted by Key3Media and published in May 2001 showed that, '56% of NPU users intend to use a *classification co-processor* to augment the capabilities of their NPU.'" (emphases added) (available at **http://www.techonline.com/community/ed_resource/feature_article/21167_PM2843515061EU**). As known in the art, "Classification processing refers to the identification and classification of individual protocol data units (PDUs) in communication traffic moving through a network." (Misha Nossik, "Optimizing Network Processing With Deep Packet Classification" April 1, 2002) (available at **http://www.reed-electronics.com/ecnmag/article/CA217341?filename=ECN20020401ec24wb104_.xml**). As the term "classification processor" was known in the art at the time of applicants filing, applicants respectfully request that this rejection of these claims be withdrawn.

## VI. REJECTIONS UNDER 35 U.S.C. §112, second paragraph

Claims 3, 6-7, 16-17, 29-30, 38, and 41 were rejected under 35 U.S.C. § 112, second paragraph, for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. With this response, claims 3 and 41 have been amended for clarity. With respect to claim 3, Applicants respectfully submit that the boundary separating the processor and the co-processor, as described throughout the specification, may include a physical or logical boundary, and have amended the claim to more clearly define this distinction. With respect to the remaining claims, claims 6, 16, and 29 were rejected because the Examiner noted a CAM cannot be a processor, and claims 7, 17, 30, and 38 were rejected because the Examiner noted the term "classification processor" is not known in the art. As previously discussed, Applicants respectfully disagree with both of these assertions. Applicants submit that claims 6-7, 16-17, 29-30, and 38 should be allowed for at least the similar reasons set forth above and respectfully request that these rejections of these claims be withdrawn.

## VII. REJECTIONS UNDER 35 U.S.C. § 102(b)

Independent claims 1, 11, 24, and 34 were rejected under 35 U.S.C. § 102(b) as being anticipated by Rutman. With this response, independent claims 1, 11, 24, and 34 have been amended for clarity. Support for these amendments may be found in the specification. No new matter has been added.

Independent claim 1, as amended, relates to a "packet processing system." The system includes: "a processor; a co-processor separated from said processor by a boundary; and an interface coupled with said processor and said co-processor and operative to bridge said boundary , said interface including: a memory coupled with said processor and said co-processor, said memory having at least two read/write ports for reading and writing data to said memory wherein said processor is coupled with one of said at least two ports and said co-processor is coupled with the other of said at least two ports; and control logic coupled with said at least two read/write ports; wherein said processor stores data intended for said co-processor to said memory and reads data stored by said co-processor from said memory independent of said co-processor; said co-processor stores data intended for said processor to said memory and reads data stored by said processor from said memory independent of said processor; and said control logic operative to facilitate the reading of said stored data by said processor and said co-processor; and wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously."

Independent claim 11, as amended, relates to an "interface for coupling a processor to a co-processor across a boundary, said processor and said co-processor being separated by said boundary." The interface includes: "a memory coupled with said processor and said co-processor, said memory having at least two read/write ports for reading and writing data to said memory wherein said processor is coupled with one of said at least two ports and said co-processor is coupled with the other of said at least two ports; and control logic coupled with said at least two read/write ports; wherein said processor stores data intended for said co-processor to said memory and reads data stored by said co-processor from said memory independent of said co-processor; said co-processor stores data intended for said processor to said memory and reads data stored by said processor from said memory independent of said processor; and said control logic operative to facilitate the reading of said stored data by said processor and said co-

processor ; and wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously"

Independent claim 24, as amended, relates to a "method of interfacing a processor with a co-processor across a boundary, said processor and said co-processor being separated by said boundary." The method includes: "(a) receiving first data from said processor via a first interface; (b) storing said first data in a memory; (c) signaling said co-processor that said first data has been stored; (d) receiving a read command from said co-processor via a second interface; and (e) providing said first data to said co-processor via said second interface across said boundary ; and wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously."

Independent claim 34, as amended, relates to an "apparatus for facilitating communications between a first processor and a second processor." The apparatus includes: "a dual port memory coupled with said first processor via first interface and said second processors via a second interface, and operative to act as a message buffer between said first processor and said second processor; control logic coupled with said dual ported memory and operative to detect communications by one of said first and second processors and inform the other of said first and second processors of said communications; and wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously."

Rutman discloses, "A special type of random access memory referred to as video random access memory (VRAM) is used through to provide multiple access to the memory in a timely manner. The VRAM is characterized by a random access port which enables random accessing to the memory array and a serial port comprising a shift register for outputting a large group of bits of data, such as pixels representative of a scan line of a video image, which are rapidly output by the memory. In the present invention, the VRAM is utilized in a different manner to provide more efficient use of memory without degradation in system performance. The VRAM provides for communications between processors as well as the memory utilized by the coprocessor for storage of code and data. Communications between processors is performed through the serial port; therefore, data is communicated via blocks of data transfers minimizing the frequency of access to the memory array. The co-processor, which utilizes the memory for processing and code storage, communicates with the memory through the random access port in order for the co-processor to perform its functions in a timely manner. The co-processor will

only be interrupted in its access of the memory when it is determined that blocks of data are to be transferred into the or out of the memory via the serial port." *See* Rutman, Abstract.

Rutman at least fails to disclose "wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously," as required by claims 1, 11, 24, and 34. In contrast, the system of Rutman includes a dual ported VRAM having a shift register and a memory array. A main processor utilizes the serial port of the VRAM to write data to the shift register, while a co-processor utilizes the random access port of the VRAM to access the memory array. *See* Rutman, col. 3, ll. 25-65. Rutman specifically discloses that the co-processor will, "be interrupted in its access of the memory when it is determined that blocks of data are to be transferred into the or out of the memory via the serial port." *See* Rutman, Abstract.

For at least these reasons, claims 1, 11, 24, and 34, as amended, are patentable over Rutman. Accordingly, Applicants respectfully request that these rejections of these claims be withdrawn.

Dependent claims 2-5, 8-9, 12-15, 18-19, 22-23, 25-28, 31, 35-36, and 39 were also rejected under 35 U.S.C. § 102(b) as being anticipated by Rutman. With this response, claim 3 has been amended for clarity. This amendment is supported by the specification, and no new matter has been added. Dependent claims 2-5, 8-9, 12-15, 18-19, 22-23, 25-28, 31, 35-36, and 39 should be allowed for the reasons set out above for the independent claims. Applicants therefore request that the Examiner withdraw this rejection of these claims.

## VIII. REJECTIONS UNDER 35 U.S.C. § 103(a)

### A. REJECTIONS OVER RUTMAN IN VIEW OF MCCORMACK ET AL.

Dependent claims 6-7, 16-17, 29-30, and 37-38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rutman in view of McCormack.

Rutman is described above.

McCormack discloses, "A graphics system for storing and editing graphic images represented by digital data, includes a frame memory for storing pixel data representing graphic images including first and second graphic objects. The pixel data is stored at addresses, each being associated with one or more graphic fragment forming the first and second graphic objects. First and second addresses are respectively associated with those of the graphic fragments

forming the first and second graphic objects. A memory controller controls writing and reading the pixel data to and from the frame memory. A fragment editor is provided to receive the pixel data read from the first address and modify the associated fragment with the received pixel data so as to form modified pixel data. An address detector detects the first address responsive to a request to read the pixel data from the first address and the second address responsive to a subsequent request to read pixel data from the second address. The detector compares the detected first and second addresses to identify an overlap of the first and second graphic objects. If an overlap is identified, the controller controls the writing of the modified pixel data to the first address before the reading of the pixel data from the second address."

As described above with respect to the rejections under 35 U.S.C. § 102(b), Rutman at least fails to disclose "wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously." McCormack et al. fails to fill the gap. McCormack discloses a graphic system which detects overlap between multiple graphic objects to ensure that each frame in the overlap is rendered properly. Nowhere does McCormack et al. disclose or suggest a system "wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously," as claimed.

For at least these reasons, claims 6-7, 16-17, 29-30, and 37-38 are patentable over Rutman in view of McCormack et al. Accordingly, Applicants respectfully request that these rejections of these claims be withdrawn.

### B. REJECTIONS OVER RUTMAN IN VIEW OF PRINCE

Claims 10, 20, 32, and 40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rutman in view of Prince.

Rutman is described above.

Prince generally describes the advantages of Synchronous RAM, such as burst synchronous SSRAMs, and includes statistics on the number of cycles required for first through fourth memory accesses.

As described above with respect to the rejections under 35 U.S.C. § 102(b), Rutman at least fails to disclose "wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously." Prince fails to fill the gap. Prince merely discloses the benefits of using various types of synchronous RAMs. Nowhere does Prince disclose or

suggest a system "wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously," as claimed.

For at least these reasons, claims 10, 20, 32, and 40 are patentable over Rutman in view of Prince. Accordingly, Applicants respectfully request that these rejections of these claims be withdrawn.

### C. REJECTIONS OVER RUTMAN

Claims 21, 33, and 41 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Rutman. With this response, claim 41 has been amended for clarity. This amendment is supported by the specification, and no new matter has been added.

Rutman is described above.

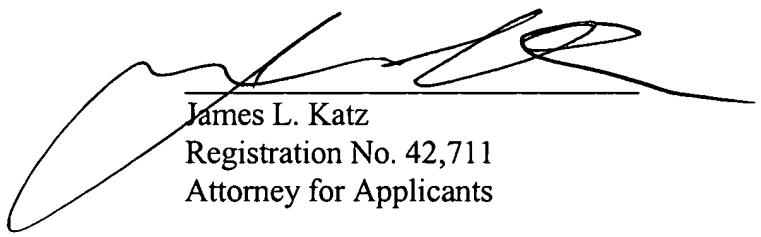
As described above with respect to the rejections under 35 U.S.C. § 102(b), Rutman at least fails to disclose "wherein said processor and said co-processor are capable of storing data to said memory substantially simultaneously."

For at least these reasons, claims 21, 33, and 41 are patentable over Rutman. Accordingly, Applicants respectfully request that these rejections of these claims be withdrawn.

## SUMMARY

Each of the rejections in the Office Action dated April 1, 2004 has been addressed and no new matter has been added. Applicants submit that all of the pending claims are in condition for allowance and notice to this effect is respectfully requested. The Examiner is invited to call the undersigned if it would expedite the prosecution of this application.

Respectfully submitted,



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